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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,232	12/06/2001	Ross A. Donelly	SNSY-A2001-007	2984

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EXAMINER
DIMYAN, MAGID Y

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,232	DONELLY ET AL.	
	Examiner	Art Unit	
	Magid Y Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgement

1. Receipt is acknowledged of the Preliminary Amendment, filed October 9, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Groeneveld et al (hereafter, Groeneveld) – U.S. Patent No. 6,230,304.

4. Referring to claim 1, Groeneveld teaches a method for placing circuit elements on an IC comprising (a) placing cells of a first circuit design by use of a non-direct timing driven layout processes (see Fig. 2; column 10, lines 23 – 37); and (b) subsequently

placing cells by use of timing driven placement processes, as claimed herein (see again Fig. 2; column 3, lines 18 – 24).

5. As per claim 2, see column 10, lines 18 – 22 which cites the global routing step that includes the optimization goals of minimizing the total net length (weighted length) of the desired circuit, and spreading the net routing evenly (i.e., minimize total weighted wiring length), as claimed herein.

6. As per claim 3, see (4) and (5) above and Fig. 2 of Groeneveld , which teach the additional limitations of routing the cells, modifying the circuit design to produce second cells of a second circuit design, and placing second cells by use of direct timing driven processes, as claimed herein.

7. As per claim 4, see (5) above, since the same rejections apply.

8. Referring to claim 5, see column 10, lines 18 – 37, which recite how routing congestion problems can be avoided (i.e., routing congestion has to be estimated so that the problem can be avoided, as claimed herein).

9. As per claim 6, see Fig. 2, steps 220 and 225 of Groeneveld, which teach how cells are sized to achieve the delay timing requirements, as claimed.

10. Referring to claims 7 and 18, see (8) above. The same rejections apply.

11. As per claims 8, 11 and 15, see above; Fig. 2; column 3, lines 15 – 33, which recite how to produce multiple placements using timing driven processes to place cells in an IC design.

12. Referring to claims 9 and 13, see (4) above; column 10, lines 18 – 22, which cite the minimization of total net lengths of the desired circuit to produce an optimum placement, as claimed.

13. As per claims 10 and 14, see (8) above. The same rejections apply.

14. Referring to claim 12 and 16, see above; Fig. 2; column 7, lines 10 – 25, which teach how to synthesize a high level description of the circuit before the cells are placed (described in detail above and in the disclosure) as claimed herein.

15. As per claim 17, see (9) above, since the same rejections apply.

16. Referring to claims 19 and 20, see above, and Abstract; Fig. 1; column 20, lines 36 – 42, which cite how a computer can be used for the cell placement, as claimed herein. All the limitations claimed are disclosed in the invention, as recited above.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No. US 2002/0162085 to Zolotykh et al recites a method for resynthesizing and optimizing an IC design using a parallel processing mode for at least some of the procedures, whereby reducing the design cycle time.

U.S. Patent No. 6,564,361 to Zolotykh et al teaches a method and apparatus for optimizing an IC design that includes computing of capacities and delays, resynthesizing the IC design using local optimization procedures.

Pub. No. US 2002/0116685 to van Ginneken et al discloses a timing closure methodology for designing an IC using a computer based upon a circuit description and based upon cells, which are selected from a cell library having an associated area.

Pub. No. US 2002/0104066 to Irie cites a timing-driven layout method that realizes timing error convergence towards zero without any timing constraint file.

Pub. No. US 2001/0013114 discloses a system that creates a layout of a circuit by placing gates at specific locations in a circuit design based upon drive strengths and wireloads of gates in a circuit.

Pub. No. US 2001/0010090 to Boyle et al teaches a method for design optimization using logical and physical information.

U.S. Patent No. 6,546,541 to Petranovic et al discloses a method and apparatus for generating constraints for an IC logic logic resynthesis algorithm.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (703) 308-1354. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Magid Y Dimyan
Examiner
Art Unit 2825

myd
June 16, 2003

VUTHE SIEK
PRIMARY EXAMINER